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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,046	03/11/2004	Von-Kyoung Kim	004-8844	4971

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EXAMINER	
SIEK, VUTHE	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,046	KIM ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,23,27 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-15,23,27,31-34 and 36-38* is/are rejected.

7)☒ Claim(s) *3-4 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/798,046 filed on 3/11/2004. Claims 1-15, 23, 27 and 31-38 remain pending in the application, where claims 14-22, 24-26 and 28-30 are canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5-15, 23, 27, 31-34 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kovacs et al. (7,069,528 B2).

4. As to claims 1, 31 and 36, Kovacs et al. teach a method for determining or detecting timing violations in an arrangement of components in an IC design (Figs. 1A-C show arrangement of components in an IC design). A timing analysis is performed to determine timing violations in a plurality of timing paths. The timing violations are distinct timing paths (Fig. 2, col. 5 lines 18-67, col. 6 lines 1-3; Fig. 1b shows distinct timing paths having timing violations; note that practically an IC design could have more than two paths as shown). Figs. 1A-C describes two distinct timing paths having timing violations, timing paths 5A and 5B, they are considered as a subset of the timing paths having a common clocked device 10A. Kovacs et al. teach identifying a different set of

timing paths having timing violations (0033). Fig. 1B within the subset of the timing paths, wire 12E and wire 12F are grouped having a second common characteristic (Logic 20B, 20C) as shown in Fig. 1B. The timing violation is selected for correction (col. 6 lines 4-67; col. 7 lines 1-62). It is noted that an IC design could have a plurality of timing paths having timing violations. Although, Kovacs et al. does not teach repeating step, it would have been obvious to practitioners in the art at the timing the invention was made to repeat the process of selecting and correcting timing paths having timing violations so that all timing paths having timing violations have been corrected.

5. As to claims 2 and 33, Kovacs et al. teach the second characteristic is a sequence of devices (Devices 20B and 20C are in sequence; Fig. 1A-C).

6. As to claim 5, Kovacs et al. teach grouping wires (timing paths) for making necessary correction to meet timing paths requirements. As known to practitioners in the art, an IC design could have a plurality of timing paths. Therefore, it would have been obvious to practitioners to further group timing paths having common sequence of device elements in order to meet timing requirements.

7. As to claim 6, Kovacs et al. teach in Fig. 1A-C, the first common characteristic comprising an origin of a timing path (clocked device).

8. As to claims 7-9, Kovacs et al. teach in Fig. 1A-C the first common characteristic comprising a destination of a timing path (clocked device); inclusion of a first block in a timing path (clocked device); inclusion of a first net in a timing path (wire 12C).

9. As to claims 10-11, Kovacs et al. teach eliminating timing violations from an IC design (Fig. 2). Kovacs et al. teach various examples of timing delay violations compared to selected threshold delays (col. 6, lines 4-67; col. 7 lines 1-63). The threshold delay can be selected to be higher that the expected worse case delay and lower that the delay value that would guarantee a timing violation. These teachings clearly anticipate the improvement of timing path includes reducing a maximum timing violation and reducing a minimum timing violation.

10. As to claims 12 and 37, Kovacs et al. teach replacement of wires or circuits to improve or eliminate timing violations of timing paths (col. 6 lines 4-67; col. 7 lines 1-63). Wires are selected and replaced by new wires for reducing timing violations; drivers or circuit components along timing paths having timing violations can be modified (sizing components, inserting components) to eliminate timing path violations. These teachings are common practice in IC design verification to meet timing requirement or to eliminate time violations.

11. As to claim 13, Kovacs et al. fabricating IC design after eliminating timing violations (col. 4 lines 15-45).

12. As to claim 14, Figs. 1A-C show preparing the IC design and thereafter performing the improvement (see also Fig. 1-2). As noted above, an IC design could have a plurality of timing paths having timings violations. In order correct all timing paths having timing violations, it would have been obvious to practitioners to repeat the step as taught by the reference.

13. As to claim 15, Kovacs et al. teach a system/method for reducing timing violations in an IC design. Therefore, IC design with corrected timing would have been manufactured.

14. As to claim 23, Kovacs et al. teach a computer system for making an IC design to conform timing requirements (Fig. 4).

15. As to claim 27, Kovacs et al. teach a computer system for making an IC design to conform timing requirements. Files of an IC design Fig. 1A-C must prepared by the system as in Fig. 4.

16. As to claim 32, as noted earlier, an IC design could have a plurality of timing paths having timing violations that could be grouped into a plurality of subsets of timing paths for making necessary correction to meet timing requirements.

17. As to claim 34, Figs. 1A-C show an IC design having a plurality of timing paths having timing violations, where the timing paths are grouped having a common characteristic for making correction to meet timing requirements. Since, an IC design could have a plurality of timing paths having timing violations that could be grouped having a common characteristic and further grouped, where the further grouped timing paths could have at least one third common characteristic for making any necessary timing correction to meet timing requirement.

18. As to claim 38, Kovacs et al. teach correcting timing violation by replacing wire with another wire. Since correcting timing violation by inserting at least one circuit element is well known in the art, the limitation is obvious to practitioners in the art at the time the invention was made.

Allowable Subject Matter

19. Claims 3-4 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest identifying a second subset of the distinct timing paths including a second plurality of timing paths, wherein each of the second plurality of timing paths includes at least one third common characteristic; and wherein a particular timing path including the at least one first characteristic and the at least one third characteristic is identified with a subset based on a prioritization of the first subset and the second subset.

Remarks

20. Applicant's remarks have been considered but not persuasive because the claims are obvious to practitioners in art. Mainly applicants argued that the reference does not teach repeating process of correcting timing path having timing violations within the group. The limitation is obvious to practitioners in the art because in order meet timing requirements, all timing paths having timing violations should be corrected. Applicants argued that the reference (Kovacs) does not teach identifying timing having a similar arrangement of circuit elements by which paths do not necessarily have any shared circuit elements, determining a correction for one of the timing paths and replicating the correction for other timing paths in the group as required by the independent claims. Examiner appreciates the comments, however such limitations are not found in the claims.

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek